Highly Uniform Trilayer Molybdenum Disulfide for Wafer-Scale Device Fabrication

Alexey Tarasov, Philip M. Campbell, Meng-Yen Tsai, Zohreh R. Hesabi, Janine Feirer, Samuel Graham, W. Jud Ready, and Eric M. Vogel*

Molybdenum disulfide (MoS_2) is a layered semiconducting material with a tunable bandgap that is promising for the next generation nanoelectronics as a substitute for graphene or silicon. Despite recent progress, the synthesis of high-quality and highly uniform MoS_2 on a large scale is still a challenge. In this work, a temperature-dependent synthesis study of large-area MoS_2 by direct sulfurization of evaporated Mo thin films on SiO_2 is presented. A variety of physical characterization techniques is employed to investigate the structural quality of the material. The film quality is shown to be similar to geological MoS_2, if synthesized at sufficiently high temperatures (1050 °C). In addition, a highly uniform growth of trilayer MoS_2 with an unprecedented uniformity of ±0.07 nm over a large area (> 10 cm^2) is achieved. These films are used to fabricate field-effect transistors following a straightforward wafer-scale UV lithography process. The intrinsic field-effect mobility is estimated to be about 6.5 ± 2.2 cm^2 V^{-1} s^{-1} and compared to previous studies. These results represent a significant step towards application of MoS_2 in nanoelectronics and sensing.

1. Introduction

The importance of two-dimensional materials has been demonstrated by the extraordinary properties of graphene,[1] which is an exciting material for basic research and very promising for a variety of applications. However, the lack of a band gap in graphene limits its use for many electronic devices. Many other two-dimensional materials exist such as transition metal dichalcogenides (TMDC) that can also be exfoliated down to atomic layer thickness.[2] The most prominent example is molybdenum disulfide (MoS_2), which has recently attracted significant attention because of its thickness-dependent electrical and optical properties.[3,4] Bulk MoS_2 is a semiconductor with an indirect band gap of 1.3 eV, whereas monolayers have a direct band gap of 1.8 eV.[3] The interest in MoS_2 as a semiconducting alternative to graphene intensified when transistors fabricated from monolayer exfoliated MoS_2 showed high on/off ratios and mobilities in the range of 0.1–10 cm^2 V^{-1} s^{-1}.[5] Possible applications have been explored including conventional integrated circuits,[6] sensors,[7–14] tunneling transistors,[15] and optoelectronics.[16–18] Moreover, MoS_2 can be transferred to any material, using methods similar to those developed for graphene. This could prove useful for applications in flexible electronics.[19–21]

Most of the studies performed so far have focused on exfoliated MoS_2 flakes.[4] However, the lateral dimensions of these flakes are very small (<100 μm) and their thickness is difficult to control. For manufacturable electronics, it is essential to have large-area material that is compatible with standard photolithography processes for high yield and reproducibility.

To solve this issue, considerable efforts have been made to synthesize large-area MoS_2 thin films using different methods. Chemical vapor deposition (CVD) using MoO_3 and sulfur has become an established method, with mobility values ranging between 0.02–17 cm^2 V^{-1} s^{-1}.[22–25] However, the resulting MoS_2 forms relatively small triangular grains by nucleation growth (<100 μm), and the formation of a wafer-scale high-quality film of controlled thickness is currently still a challenge.[23,24,26] In a different self-limiting CVD approach, Yu et al. have used $MoCl_5$ precursor instead of MoO_3 and demonstrated control over layer size, thickness and uniformity but the electrical properties of this MoS_2 are poor compared to CVD grains (the field-effect mobilities are in the range $0.003-0.03$ cm^2 V^{-1} s^{-1}).[27]

Another promising and straightforward method is to prepare a Mo-containing thin film and sulfurize it at high temperatures.[28–30] In principle, this method has the advantage of controlling the layer thickness by simply adjusting the Mo evaporation rate and time, and could potentially provide film uniformity on a wafer scale. However, a reliable transistor operation has not yet been shown.[28,29]

In this paper, we perform a temperature dependent synthesis study of large-area MoS_2 by direct sulfurization of an evaporated Mo film on a SiO_2 substrate. We first present the physical characterization results from 5 nm thick Mo samples that were

Dr. A. Tarasov, P. M. Campbell, M.-Y. Tsai, Dr. Z. R. Hesabi, J. Feirer, Prof. E. M. Vogel
School of Materials Science and Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332, USA
E-mail: alexey.tarasov@mse.gatech.edu
Prof. S. Graham
The George W. Woodruff School of Mechanical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332, USA
Prof. W. J. Ready
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332, USA

DOI: 10.1002/adfm.201401389

sulfurized at different temperatures to have a good comparison with the bulk geological MoS_2 and to study the growth process. After that, we demonstrate that our method can also reliably produce thinner MoS_2 layers with unprecedented uniformity on a large scale. We show electrical measurements obtained from 1 nm Mo samples, grown at the highest temperature (1050 °C). Finally, we investigate the effect of the contact resistance on the device performance and estimate the intrinsic field-effect mobility after subtracting the contribution from the contacts.

2. Growth and Physical Characterization

The growth process is sketched in **Figure 1**a. Highly doped silicon wafers were thermally oxidized to create a 300 nm thick SiO_2. Prior to Mo deposition, the substrate was cleaned with organic solvents and piranha solution. A thin Mo layer was deposited by e-beam evaporation at a rate of 0.3 Å s^{-1}. We deposited different thicknesses of Mo in the range 1–5 nm. The Mo films were then directly sulfurized in a furnace for 1 h in an Ar/S atmosphere at temperatures between 550 °C and 1050 °C. The best results were achieved at the highest temperature. The schematic of the sulfurization furnace is provided in Figure 1b. The sulfur vapor pressure is controlled by preheating a separate sulfur container. After evacuating the chamber, the samples were first annealed in an Ar/H_2 (4:1) atmosphere for 30 min at 300 °C to eliminate possible oxygen contamination. Meanwhile, the sulfur was preheated to 160 °C to generate a sufficient vapor pressure. Afterwards, the chamber was soaked with sulfur gas (20 mTorr) and argon carrier gas (5 Torr). The chamber was heated to the final temperature and left there for 1 h with all valves closed. The chamber was then purged with Ar and cooled down under a constant Ar flow.

To evaluate the stoichiometry of the synthetic MoS_2, we performed X-ray photoelectron spectroscopy (XPS) measurements that are summarized in **Figure 2**. In part a, Mo 3d scans are plotted for different growth temperatures of synthetic MoS_2 and for a bulk geological crystal. The Mo 3d spectra exhibit a clear doublet (Mo 3d 5/2 at 229.4 eV, Mo 3d 3/2 at 232.6 eV) along with a small S 2s peak at 226.6 eV. Similarly, the S 2p spectrum shows a doublet (Figure 2b), with the 2p 3/2 peak at 162 eV and the 2p 1/2 peak at 163.2 eV. The peaks are fitted by a Gaussian-Lorentzian cross product with a Shirley background. To obtain the stoichiometry of the sample, the peak areas are normalized using empirical relative sensitivity factors (RSFs) of 2.75 for the Mo 3d peak and 0.54 for the S 2p.[31] The stoichiometry, defined as the ratio of the normalized peak areas S 2p/Mo 3d, is plotted in Figure 2c as a function of growth temperature. The bulk value is represented by the dashed line. The stoichiometry of the grown MoS_2 clearly improves with temperature and saturates at the bulk value above 750 °C. We conclude that MoS_2 with stoichiometry equivalent to bulk can be achieved if the growth temperature is sufficiently high.

Further structural analysis is performed using Raman spectroscopy. Raman spectra of the synthetic MoS_2, made by sulfurization of a 5 nm thick Mo film at different temperatures, are depicted in **Figure 3**a (measured with a 532 nm laser). The typical MoS_2 double peak is visible around 400 cm^{-1}. The E^1_{2g} peak represents the in-plane vibrations of the Mo and S atoms, and A_{1g} denotes the out-of-plane vibrations of the sulfur atoms.[32,33] The measured E^1_{2g} position is at ~382 cm^{-1} and A_{1g} is at ~407 cm^{-1}, independent of the growth temperature. This corresponds to a peak separation Δ~25 cm^{-1} and agrees well with the previous measurements on exfoliated bulk flakes.[32,33] We find that the full-width at half-maximum (FWHM) of the E^1_{2g} and A_{1g} peaks decreases as the growth

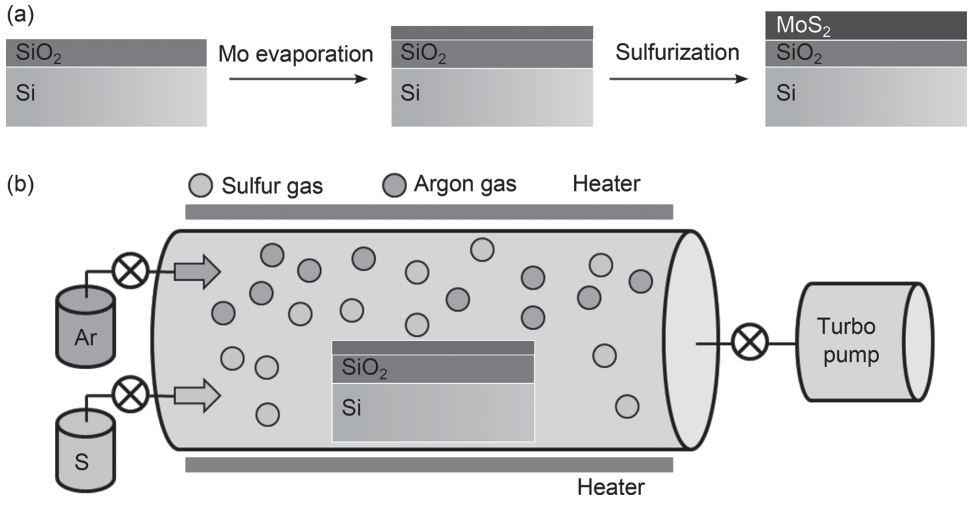

Figure 1. a) Growth process schematics. Highly doped silicon (Si) with 300 nm thermally grown SiO_2 was used as a substrate. Prior to molybdenum (Mo) deposition, the substrate was cleaned with piranha solution. Mo thin films of different thickness (1–5 nm) were deposited by e-beam evaporation at a rate of 0.3 Å s^{-1}. The Mo films were then directly sulfurized in a furnace for 1 h in an Ar/S atmosphere at temperatures between 550 °C and 1050 °C. The resulting MoS_2 layers were systematically studied using different characterization techniques. The temperature is a critical parameter and the best results were achieved above 1000 °C. b) Schematics of the sulfurization furnace. After evacuating the chamber, the samples were first annealed in an Ar/H_2 (4:1) atmosphere for 30 min at 300 °C to eliminate possible oxygen contamination. Meanwhile, a separate sulfur container was preheated to 160 °C to generate a sufficient vapor pressure. Afterwards, the chamber was soaked with preheated sulfur gas (20 mTorr) and argon carrier gas (5 Torr). The chamber was then heated to the final temperature and left there for 1 h with all valves closed. Finally, the chamber was purged with Ar and cooled down under a constant Ar flow.

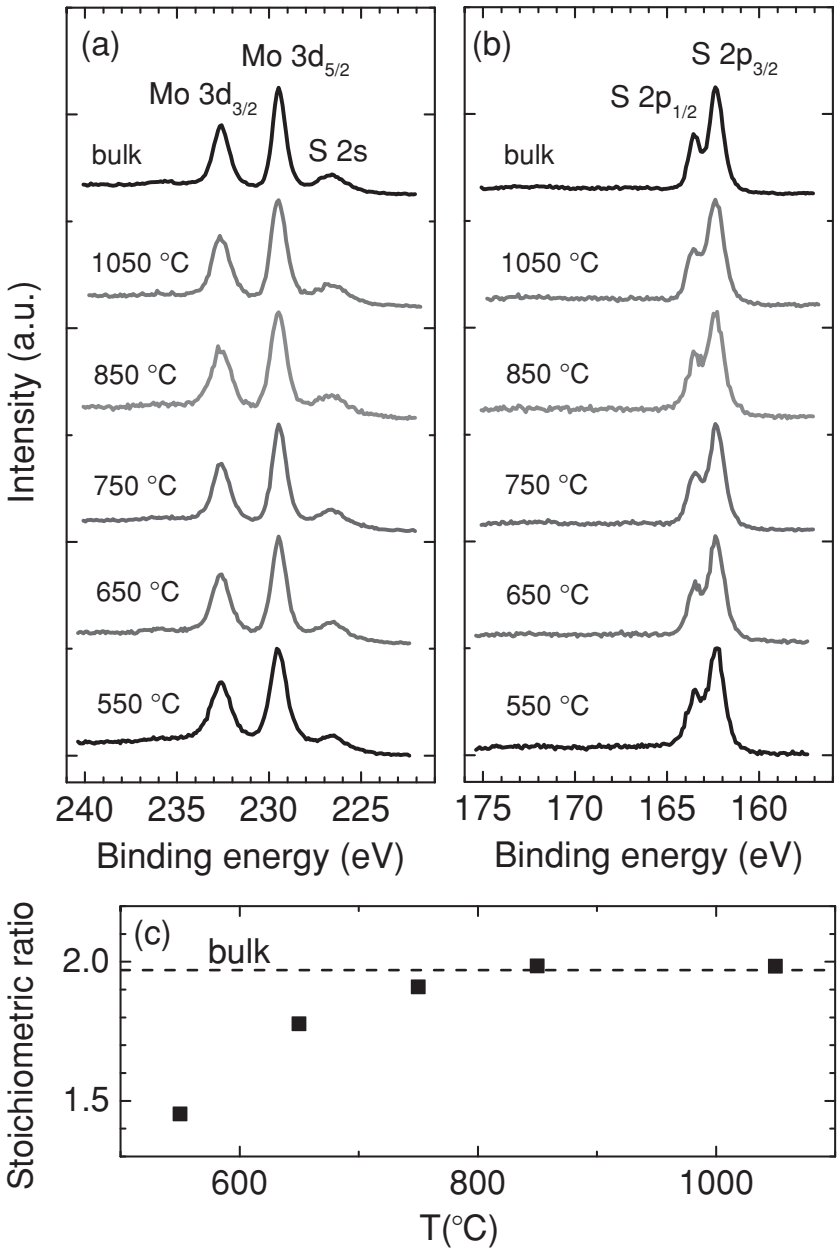

Figure 2. X-Ray photoelectron spectroscopy data (XPS) from a 5 nm Mo layer after sulfurization at different growth temperatures, compared with geological bulk crystal. The typical Mo 3d doublets a) and S 2p doublets b) are clearly pronounced and very similar to geological bulk crystal. The Mo 3d and S 2p peaks were fitted using a method described in the text. c) The fitted S 2p peak area was divided by the Mo 3d area to estimate the stoichiometric ratio as a function of temperature. The ratio increases with temperature and reaches the bulk value above 750 °C.

temperature rises (Figure 3b). The peak width reaches the bulk values (indicated by dashed lines) only above 1000 °C. This shows that the structural quality of the synthesized MoS_2 greatly improves at higher growth temperatures and is similar to geological MoS_2 if grown at temperatures >1000 °C. We also observe that the relative intensity of the MoS_2 signal vs Si background peak at 520 cm^{-1} increases with temperature. Similarly, Laskar et al.[29] showed that the intensity of the MoS_2 peaks grown on sapphire increases with rising growth temperature. The authors attributed this effect to the improved structural quality of the material.

Crystallinity is another crucial factor determining the quality of the synthetic films. Because our films are very thin (≈10 nm), it is difficult to measure the crystal structure using standard in-plane X-ray diffraction. We therefore employed grazing incidence X-ray diffraction (GIXRD) to access the crystal structure of the material. The X-ray incidence angle was set to 0.5° to optimize the signal from the thin film. Grazing incidence X-ray diffraction spectra from synthetic samples and the bulk crystal are compared in **Figure 4**a. All samples (including the bulk crystal) show a prominent peak at around $2\theta = 14.4°$, which corresponds to the (0002) crystal orientation (hexagonal MoS_2). Figure 4b focuses on the enlarged region around the dominant (0002) peak. We find that both the peak position and the FWHM improve at higher temperature. The peak positions 2θ are plotted in part c against the growth temperature. It is evident that above 1000 °C the peak position of the synthetic film reaches the bulk value (dashed line). The downshift from the ideal peak position at lower temperatures indicates lattice expansion as a result of structural imperfections.[34] As the temperature rises, the MoS_2 structure relaxes and the peak position reaches the standard value. In Figure 4d, the FWHM decreases with temperature and approaches the bulk value above 1000 °C. A narrower peak width suggests a larger grain size. Based on these observations, we conclude that the crystal orientation and structural quality of synthetic MoS_2 can be improved at higher temperatures, and is comparable to the bulk crystal.

The presence of the (0002) peaks at 14.4° implies that both the bulk sample and synthesized films have planes with the correct interlayer stacking distance. However, in order to observe the (0002) planes at 2θ = 14.4° with a fixed incident beam angle of 0.5° in the GIXRD setup, the detector angle must be 13.9° with respect to the substrate. The (0002) planes must also be aligned such that the incident and diffracted beam angles are both equal, with respect to the diffracting planes, in this case 7.2° (14.4°/2). One possible reason for such misalignment of a few degrees could be the formation of energetically favorable ripples or waves on the MoS_2 surface.[35] This is also consistent with our scanning transmission electron microscope (STEM) images that will be presented below. A more detailed comparison of the microstructure of geological and synthesized MoS_2 will be performed in future studies.

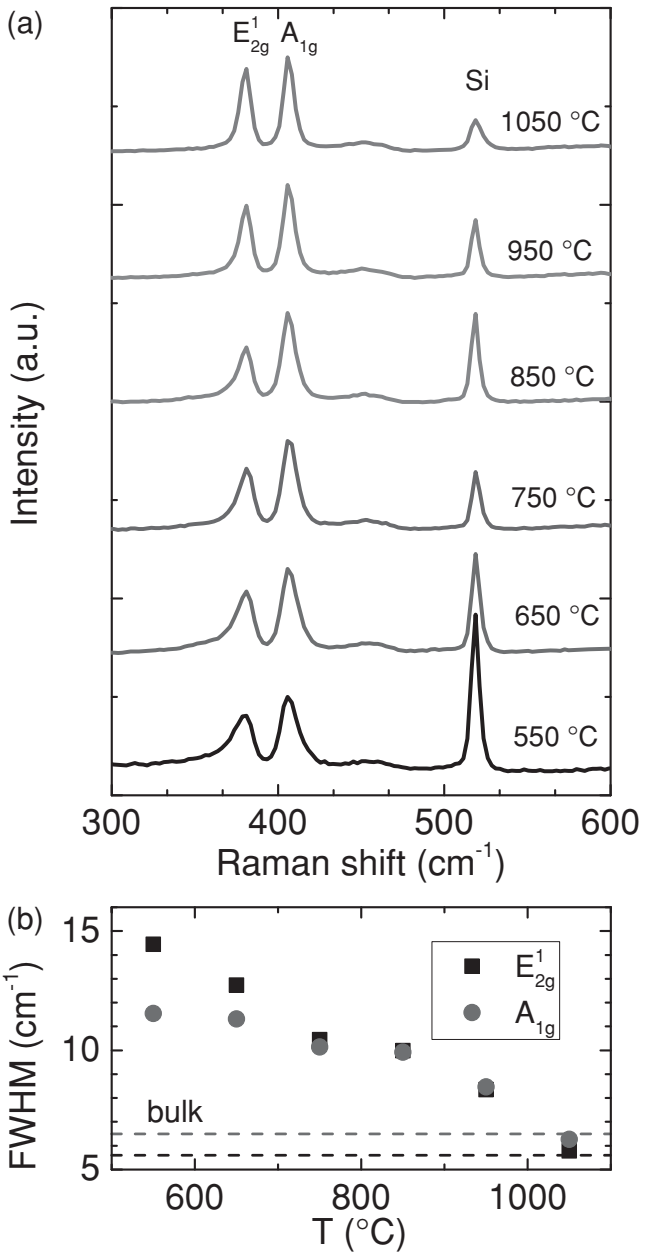

Figure 3. a) Raman spectra from a 5 nm Mo layer after sulfurization at different growth temperatures (532 nm laser). Typical MoS_2 double peak is visible around 400 cm^{-1}. The E^1_{2g} peak represents the in-plane vibrations of Mo and S atoms, and A_{1g} denotes the out-of-plane vibrations of sulfur atoms. The spectra were normalized to the A_{1g} peak intensity and are shown vertically offset for clarity. The MoS_2 peaks become narrower with increasing growth temperature, and their intensity relative to the Si peak increases. b) The full-width at half-maximum (FWHM) of the E^1_{2g} and A_{1g} peaks as a function of temperature. The peak width decreases as the temperature goes up and reaches the bulk values (dashed lines) only above 1000 °C. This shows that the structural quality of MoS_2 strongly improves at higher growth temperatures.

So far we have only studied relatively thick MoS_2 (≈10 nm) based on 5 nm thick Mo layers. This helped us optimize the growth process and compare the physical properties with the bulk geological material. However, most of the recent work has dealt with single-layer or few-layer MoS_2. In the following we demonstrate that our method can also provide thinner layers of highly uniform MoS_2 in a well-controlled way. To do so, we evaporated 1 nm Mo and sulfurized it at the highest possible temperature (1050 °C, limited by the furnace). Note that we did not intentionally oxidize the 1 nm Mo film before the sulfurization but it naturally forms an oxide (MoO_x) either during deposition or exposure to atmosphere. Then, we fabricated dual-gated field-effect transistors using a wafer-scale UV lithography process to study the electrical properties of the material.

Figure 5a shows a photograph of a wafer die after device fabrication. This thickness of Mo (1 nm) is expected to give approximately 2 nm or 3 layers of MoS_2. To study the film uniformity, we performed Raman measurements at 15 different positions across the whole sample area (Figure 5b). All spectra align perfectly on top of each other. The separation between the characteristic MoS_2 peaks (E^1_{2g} and A_{1g}) is 23.53 ± 0.04 cm^{-1} (Figure 5c), which indeed corresponds to 3 layers of MoS_2.[32,33] Around a trilayer MoS_2 thickness, a change in Raman peak separation by ≈1 cm^{-1} corresponds to a thickness difference of 1 monolayer (ML) or ≈0.65 nm. We show a uniformity of ≈0.04 cm^{-1} which corresponds to ≈0.04 ML. As a conservative estimate, our film uniformity is 3 ML ±0.1 ML across the entire area of the chip (>10 cm^2). Assuming a monolayer thickness of ≈0.65 nm, this uniformity approximately corresponds to ±0.07 nm. For comparison, the CVD growth of MoS_2 produces films with large variations in thickness from monolayer to >4 layers over an area <1 cm^2.[23] We conclude that the film uniformity presented here is an order of magnitude better than that of CVD grown MoS_2.

We also collected small-area Raman maps across the area of a transistor (in 5 μm steps). **Figure 6**a provides an optical microscope image of a single transistor. The inset shows the peak separation E^1_{2g} – A_{1g} at 36 different positions. The mean value is again very close to 23.5 ± 0.1 cm^{-1} and extremely uniform across the area of the transistor. In addition, cross-sectional scanning transmission electron microscope images (STEM) were performed on a transistor after fabrication to resolve the layered structure of the material (Figure 5b–d). The sample was prepared using a focused ion beam (FIB) system prior to imaging (see Experimental Section for details). In Figure 6b, a lower magnification image of the contact region is shown, acquired in transmitted electron mode (bright-field). The image reveals a thin layer of MoS_2 between the SiO_2 substrate and the titanium and gold (Ti/Au) contacts. At higher magnification (c), good stacking of 3 MoS_2 layers is resolved (trilayer). Molybdenum layers appear darker than the sulfur layers because of the higher atomic number of Mo. The total MoS_2 thickness is around 2 nm. This value matches surprisingly well with our expectations and the Raman data. The same area is also shown in atomic number contrast mode (part d), with the color scale inverted (dark-field, Mo appears lighter than S).

3. Electrical Measurements

Now we turn our attention to the electrical properties of the trilayer MoS_2. Using UV lithography, we fabricated several samples with hundreds of transistors each. The transistor

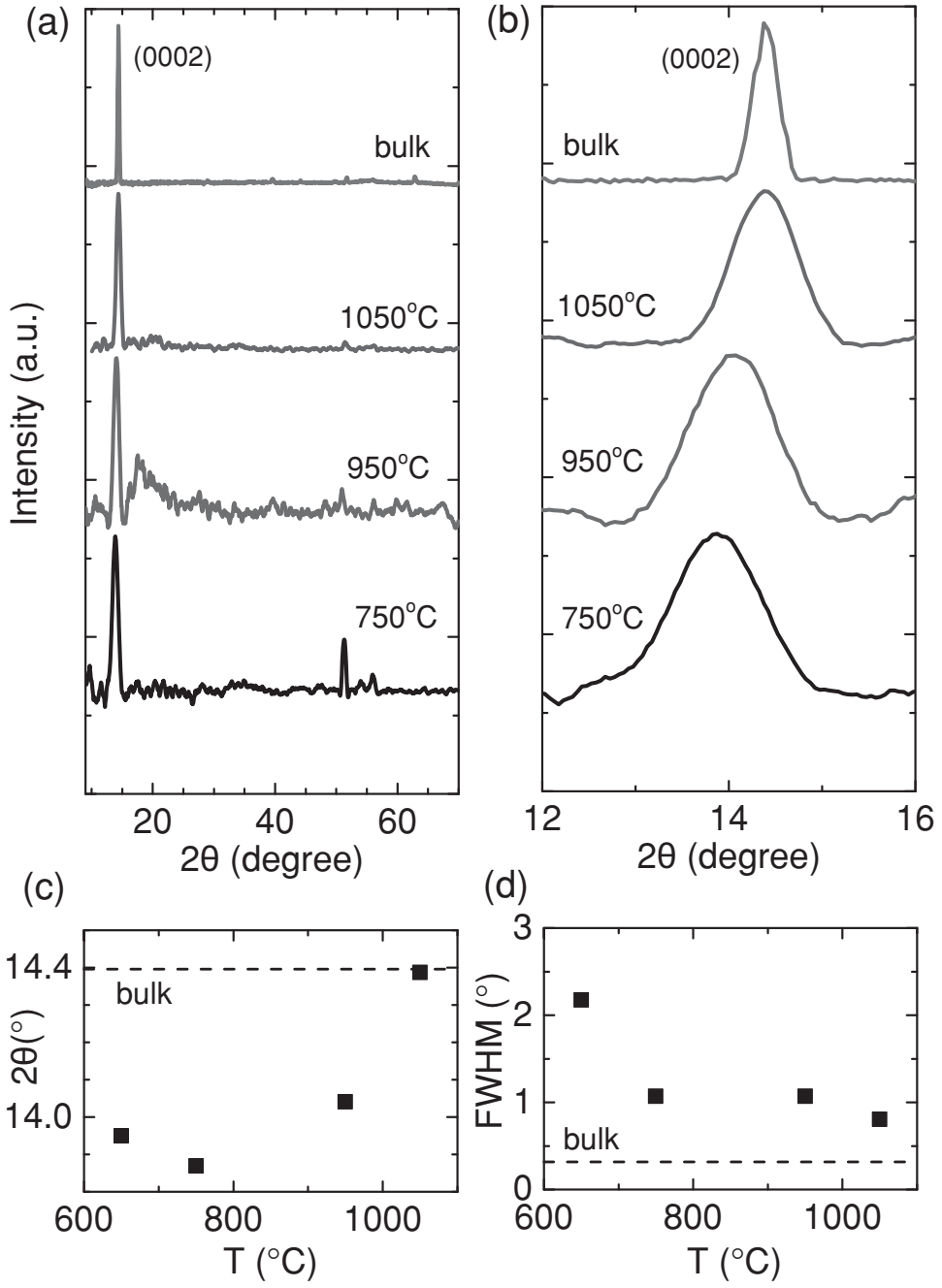

Figure 4. a) Grazing incidence X-ray diffraction (GIXRD) data from 5 nm Mo layers after sulfurization at different growth temperatures, compared with geological bulk crystal. All samples show a prominent peak at around 14.4°, which corresponds to the (0002) crystal orientation (hexagonal MoS_2). b) Enlarged region around the dominant (0002) peak. Both the peak position and the FWHM improve with temperature. c) Peak position 2θ vs temperature T, extracted from (b). The 2θ downshift from the ideal value at lower temperatures is attributed to the lattice expansion due to structural imperfections. The peak position reaches the bulk value (dashed line) above 1000 °C. d) FWHM decreases with temperature and approaches the bulk value (dashed line) above 1000 °C. Narrower peak width suggests a larger grain size.

channels were defined by dry etching the MoS_2 with an SF_6/O_2 mixture. The source and drain contacts were formed by e-beam evaporation of 30 nm titanium (Ti) and 30 nm of gold (Au). Several tens of back-gated transistors were first tested after this step. The yield was 100%. Then, 30 nm of alumina (Al_2O_3) were grown by atomic layer deposition (ALD) at 250 °C, followed by the evaporation of a Ti/Au top gate electrode. 13 transistors were measured again after ALD in a dual-gated configuration (**Figure 7**a). All measurements were done using a Keithley 4200-SCS parameter analyzer and a CascadeMicrotech probe station at room temperature and ambient conditions.

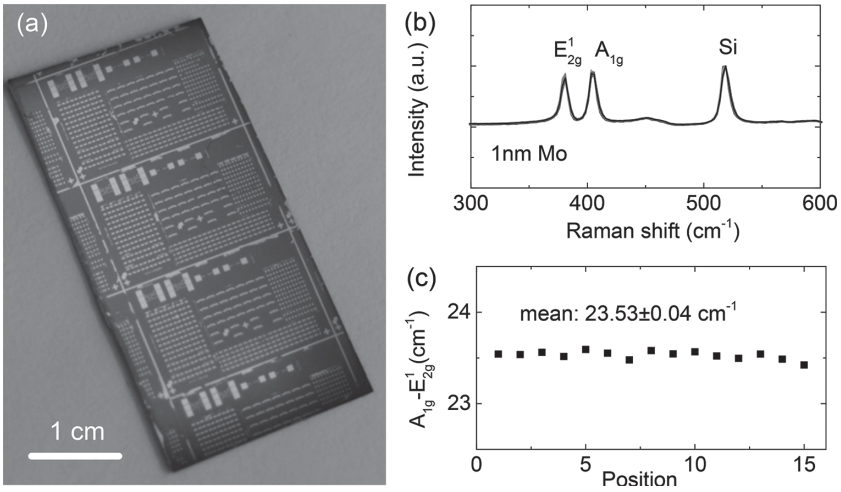

Figure 5. The thinnest MoS_2 sample (1 nm Mo, sulfurized at 1050 °C) was used for device fabrication following a wafer-scale UV lithography process. a) The optical image shows a wafer die after device fabrication. b) Raman spectra from 15 different areas of the sulfurized wafer align perfectly on top of each other. c) The peak separation $A_{1g} - E^1_{2g} \approx 23.53 \pm 0.04$ cm^{-1} is smaller than for the bulk material (25 cm^{-1}) and corresponds to 3 layers of MoS_2. The thickness uniformity is ~0.1 monolayers (or ~0.07 nm) across the whole wafer.

In the following, we focus on a representative data set obtained from 13 dual-gated transistors. The transistors were randomly chosen from the entire die area of ≈10 cm^2 (see Figure 5a). Figure 7a shows the schematic of a dual-gated transistor and the measurement circuit. In part (b), the measured drain current I_d is plotted vs the applied back-gate voltage V_{bg} at fixed source-drain voltage $V_{ds} = 1$ V (transfer curve). The top-gate is grounded ($V_{tg} = 0$ V) to avoid spurious coupling effects between the top-gate and the back-gate that have been observed if the top gate was left floating.[36] The transfer curve on a semi-logarithmic scale (left vertical axis) shows both gate sweep directions, indicated by arrows. The hysteresis is negligible because the top dielectric protects the MoS_2 channel from environmental factors such as humidity and oxygen, as has been previously studied.[37–40] The linear transfer curves (right axis) compare one sweep direction for 2 different transistors, FET 1 (solid symbols) and FET 2 (empty symbols). Both curves align very well on top of each other. These transistors are several centimeters apart, suggesting good film uniformity. The output curves I_d vs V_{ds} are plotted in Figure 7c for different back-gate values. The curves are linear and symmetric around $V_{ds} = 0$ V, usually indicative of Ohmic behavior. The applied drain-source voltages $V_{ds} \leq 1$ V are well inside the linear regime of operation. However, it has been shown that a linear output characteristics can occur due to thermally assisted tunneling in atomically thin materials even if a significant Schottky barrier is present at the semiconductor-metal interface.[41] The maximum drain currents measured here are comparatively low, suggesting a strong contribution from the contact resistance, which can dramatically lower the drain current.[26,41]

The contact resistance is mainly determined by two key factors: (1) a Schottky barrier as a result of the work function difference between the semiconductor and the contact metal; (2) a significant number of interface states which is influenced by the material quality, fabrication process, sample cleanliness etc.[26,41–43] High contact resistance is a major issue for transistors based on two-dimensional semiconductors because the source/drain regions are not heavily doped like in conventional semiconductors. Well-established techniques such as ion implantation are difficult to use because of the atomically thin structures. Therefore, several systematic studies have been conducted to minimize the Schottky barrier formation by using low work function metals such as titanium[4] and scandium,[41] or using a tunnel barrier (MgO[43] or TiO_2[44]) between a ferromagnetic metal and MoS_2. Contact doping with nitrogen dioxide, potassium, and polyethylenimine has also been demonstrated in TMDCs.[4] Despite this progress, the influence of the contact resistance remains an issue and it is important to have a reliable method to quantify its contribution.

Here, we use dual-gated measurements to extract the contact resistance, similar to the approach presented by Liu et al.[26] The method is based on the fact that the top-gate only modulates the MoS_2 channel but not the contact leads (see Figure 7a). As a result, there is a top-gate independent extrinsic resistance associated with the contacts. This extrinsic resistance R_{ext} consists of both the contact resistance and the MoS_2 resistance under the contact leads. The total resistance of a device with 2 contacts R_{tot} is a sum of the channel resistance and twice the extrinsic resistance $R_{tot} = R_{ch} + 2R_{ext}$. In the following, we show that R_{ext} can dominate the total resistance, depending on the applied gate voltage. To do so, we sweep the top-gate voltage at different back-gate values and measure the drain current. The data is plotted in **Figure 8** as a scatter plot (a) and as a contour

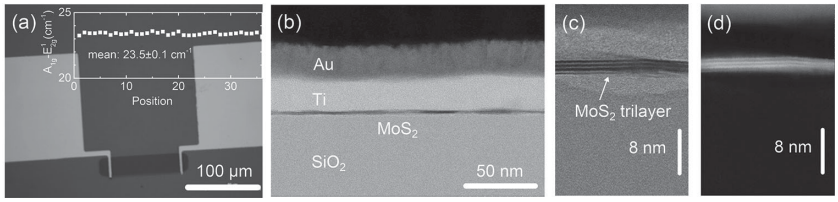

Figure 6. a) An optical image of a trilayer MoS_2 transistor with Ti/Au contacts before the top-gate deposition. Inset: Raman maps were taken across the area of a transistor. The peak separation was $A_{1g} - E^1_{2g} \approx 23.5 \pm 0.1$ cm^{-1}, showing excellent uniformity. b–d) The thickness was confirmed by cross-sectional STEM, performed on a transistor after fabrication. b) A bright-field (BF) image across the contact region in (a) shows a thin MoS_2 layer between the SiO_2 substrate and the Ti/Au contact material. MoS_2 appears darker than SiO_2 or Ti because of the higher atomic number of Mo. c) A BF image at higher magnification reveals good stacking of 3 layers of MoS_2 (Mo layers are darker than S). d) The same area is also shown as a dark-field image. The total MoS_2 thickness is around 2 nm. This matches well with our expectation because we deposited 1 nm Mo which should yield 3 layers of MoS_2 after sulfurization.

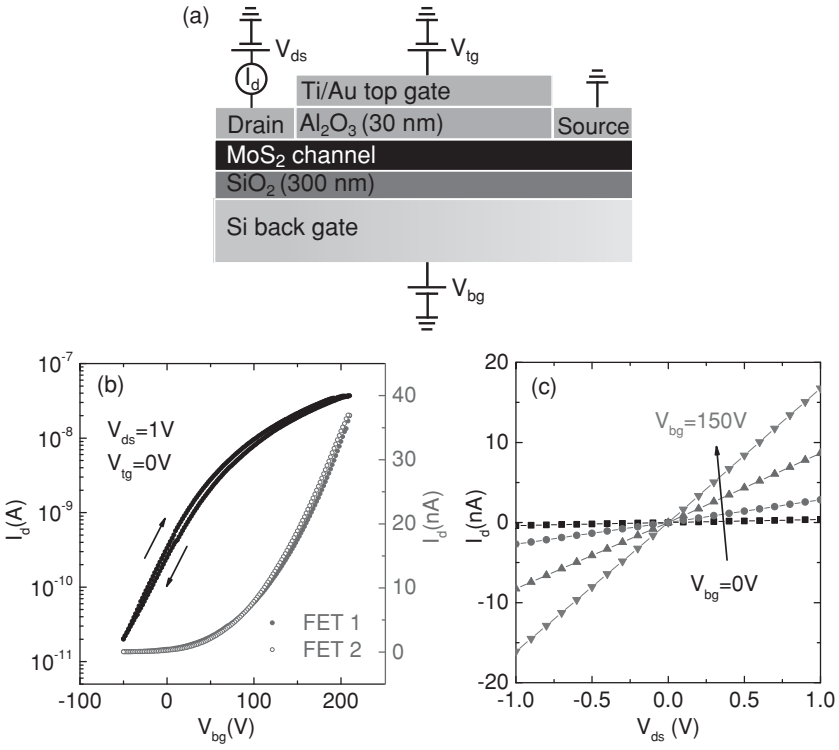

Figure 7. a) Schematics of a dual-gated trilayer MoS_2 transistor (not to scale). The drain-source voltage V_{ds} is applied to the Ti/Au contacts on top of MoS_2. The channel is covered with 30 nm Al_2O_3 and a Ti/Au top gate electrode. The drain current I_d through the MoS_2 channel is measured as a function of the back gate voltage V_{bg} and the top gate voltage V_{tg}. b) Drain current I_d through the MoS_2 channel as a function of the applied back-gate voltage V_{bg} (transfer curve) at constant drain-source voltage $V_{ds} = 1$ V, with the top-gate grounded ($V_{tg} = 0$ V). The transfer curve on the semi logarithmic scale (left vertical axis) shows both gate sweep directions, indicated by arrows. The hysteresis is negligible. The linear transfer curves (right axis) compare one sweep direction for two different transistors, FET 1 (solid circles) and FET 2 (empty circles). Both curves align very well on top of each other. The transistors are several centimeters apart, suggesting high uniformity of the film. c) The output curves I_d vs V_{ds} are linear and symmetric around $V_{ds} = 0$ V (Ohmic behavior). The applied drain-source voltages $V_{ds} \leq 1$ V are well inside the linear regime of operation.

plot (b). The top-gated transfer curves in (a) are plotted on a linear scale and completely saturate at positive $V_{tg} = 7$ V, indicated by the dashed line. In this regime, the top-gate still modulates the channel resistance R_{ch} but once $R_{ch} \ll R_{ext}$, the total resistance is given by $R_{tot} \approx 2R_{ext}$, and the drain current saturates. Similar current saturation was reported by Liu et al. in dual-gated transistors made from CVD-grown monolayer MoS_2 grains.[26] The authors did not show top-gate sweeps at different back-gate values but it is clear from Figure 8a that the global back-gate can still modulate R_{ext} and R_{tot}, thus the drain current increases with V_{bg} even at $V_{tg} = 7$ V.

The contour plot in Figure 8b shows the drain current I_d (grayscale) as a function of both V_{bg} (horizontal axis) and V_{tg} (vertical axis). The lower left corner corresponds to the depletion region where the current is small, and the upper right part is the accumulation region where the current is large. The lines of constant I_d values (thin black lines) evolve from a small slope $s = \partial V_{tg} / \partial V_{bg} \approx 0.05$ (white line and number) in the lower region ($V_{tg} < 2$ V) to a much steeper slope $s \approx 2.0$ above $V_{tg} > 2$ V (compare with the current saturation in Figure 8a). This slope s corresponds to the capacitive coupling ratio between the back-gate capacitance and the top-gate capacitance $s = C_{bg} / C_{tg}$.[45,46] Assuming that I_d is determined only by the MoS_2 channel, the parallel plate capacitor model predicts the coupling ratio to be $\frac{C_{bg}}{C_{tg}} = \frac{\varepsilon_{bg} t_{tg}}{\varepsilon_{tg} t_{bg}} \approx 0.05$, with $\varepsilon_{tg} \approx 8.5$ being the relative permittivity of Al_2O_3 (extracted from CV measurements), $\varepsilon_{tg} = 3.9$ the relative permittivity of SiO_2, $t_{bg} = 300$ nm the SiO_2 thickness, and $t_{tg} = 30$ nm the Al_2O_3 thickness (the device cross-section is depicted in Figure 7a). This value is in excellent agreement with the slope in the lower region, meaning that the current is determined by the channel. The steep slope in the upper part of the contour plot can be explained by the gating of the contact leads. Because the gate coupling from the top-gate is dramatically reduced for this extrinsic resistance (meaning a small C_{tg}), the gate capacitance ratio increases, resulting in a large slope $s = C_{bg}/C_{tg} \approx 2.0$. This means that the upper region is dominated by the extrinsic resistance.[45,46] Therefore, we can distinguish between 2 different regimes based on the magnitude of the slope: the channel-dominated regime in the lower part of the contour plot where the slope is small, and the contact-dominated (or extrinsic regime) in the upper region where the slope is large.

Using the saturation current at $V_{tg} = 7$ V in Figure 8a, we can now estimate the extrinsic resistance as a function of the back-gate voltage by applying $R_{ext} = V_{ds}/2I_d$. The results are plotted in Figure 8c. We observe a reduction of the extrinsic resistance by two orders of magnitude over the back-gate range measured here, similar to previous studies that used TLM structures[47] or four-point measurements[48] to extract the effect of the contacts. Even at high back-gate values, the extrinsic resistance can be as high as 10 MΩ, which explains why the maximum drain currents are relatively low in our back-gated measurements (Figure 8d).

4. Discussion of Mobility

In the following, we subtract the influence of the extrinsic resistance from the transfer curves and estimate the intrinsic field-effect mobility to understand the true potential of our MoS_2 films. **Figure 9**a shows the same transfer curves as in Figure 7b after subtracting the extrinsic resistance $2R_{ext}$. The corrected maximum drain current $I_{d,corr}$ has increased by approximately 4 times, emphasizing the large influence of the contacts. From the slope of these transfer curves, the intrinsic field-effect mobility μ_{FE}^{int} can be estimated using the following expression

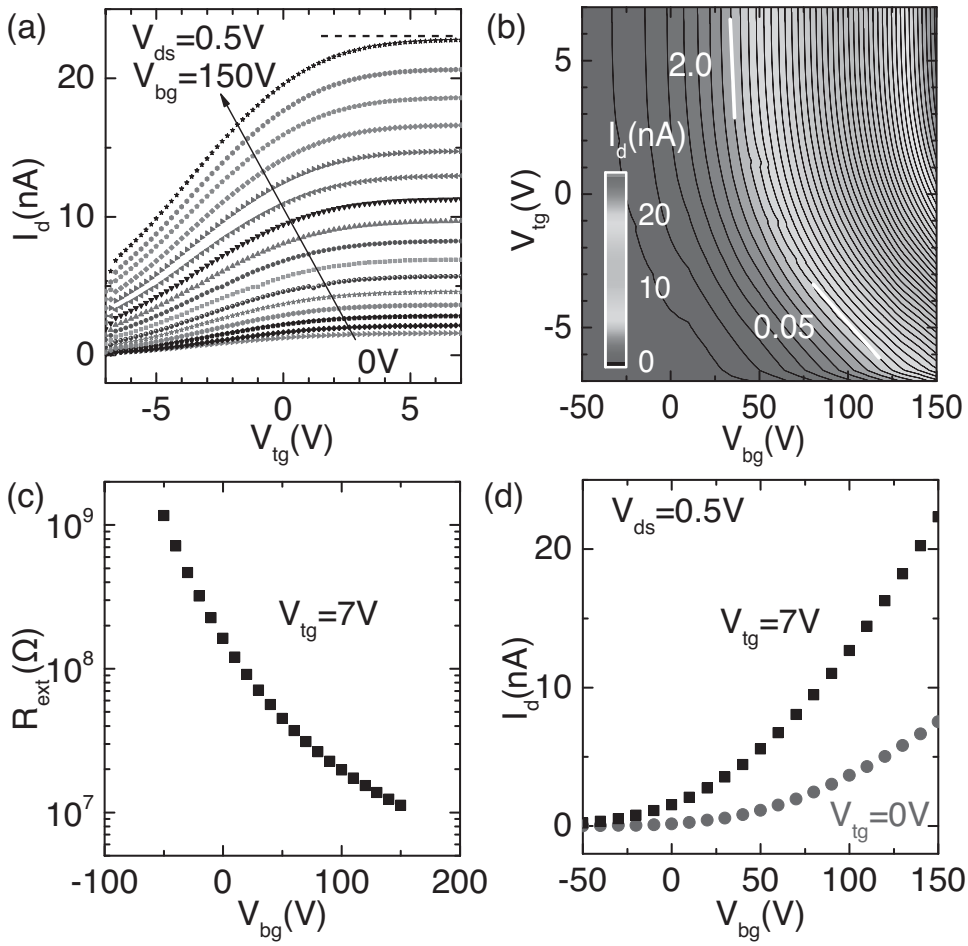

Figure 8. Dual-gated measurements were performed to study the extrinsic resistance R_{ext}. a) Drain current I_d vs top-gate voltage V_{tg} at different back-gate values V_{bg} (linear scale). The current saturates at positive V_{tg} because the top-gate only modulates the channel but not the contacts. In this regime, the extrinsic resistance R_{ext} dominates the total resistance $R_{tot} = V_{ds} / I_d \approx 2R_{ext}$ (dashed line). b) Contour plot of I_d (grayscale) vs V_{tg} and V_{bg} also shows 2 different regimes: the channel-dominated regime in the lower part, where the slope is small ($s = 0.05$, solid line), and the contact-dominated (or extrinsic regime) in the upper part, where the slope is large ($s = 2.0$). c) Using the saturation current value at $V_{tg} = 7$ V from part a), the extrinsic resistance $R_{ext} = V_{ds} / 2I_d$ can be extracted as a function of the back-gate voltage V_{bg}. d) Unlike the top-gated measurement, I_d vs V_{bg} does not show current saturation because the global back gate also modulates the extrinsic resistance.

$$\mu_{FE}^{int} = \frac{dI_{d,corr}}{dV_{bg}} \cdot \frac{L}{WC_{bg}V_{ds}} \quad (1)$$

with $\frac{dI_{d,corr}}{dV_{bg}}$ being the transconductance (derivative of the transfer curve), $L = 100$ µm the channel length, $W = 10$ µm the channel width, $C_{bg} \approx 10^{-4}$ F m^{-2} the estimated back-gate capacitance per unit area, and $V_{ds} = 1$ V the source-drain voltage. The results are summarized in Figure 9b for all measured transistors. The mean value is 6.5 ± 2.2 cm^2 V^{-1} s^{-1}. We stress that the transistors are made from a continuous and extremely uniform trilayer MoS_2 (3 ML ± 0.1 ML) over a large area of a die (>10 cm^2).

The correct characterization methodology for extracting mobility of 2D materials is a matter of debate in the literature. Variations in extraction methodology and contact resistance result in variations of reported mobility values. To discuss our results in the context of recent work, we have summarized previously reported room temperature mobility values in **Table 1**. The left part of Table 1 focuses on the results obtained with exfoliated flakes of different thickness and typical lateral dimensions <100 µm. Most of the studies used single-layer (sl) or bilayer (2l) flakes and the reported mobility ranges from 0.1 to 80 cm^2 V^{-1} s^{-1}, probably depending on the material quality and fabrication details. We are aware of 2 studies that used trilayer MoS_2 flakes (3l), which would be a good comparison to the present work. Park et al.[37] reported a mobility of 5–7.6 cm^2 V^{-1} s^{-1} for the 3l flakes, while Ghatak et al.[49] estimated 10 cm^2 V^{-1} s^{-1}, in good agreement with our results. A comprehensive thickness-dependent study on multilayer MoS_2 reported values around 20–30 cm^2 V^{-1} s^{-1} for their thinnest samples (≈2 nm) with scandium contacts.[41,50] The authors also found that the mobility reaches the maximum value around 10 nm thick exfoliated MoS_2 flakes (>100 cm^2 V^{-1} s^{-1}), before it decreases again above 10 nm.[4,41,50] Overall, our mobility is on the same order of magnitude as the values reported for 2–3 nm thick exfoliated

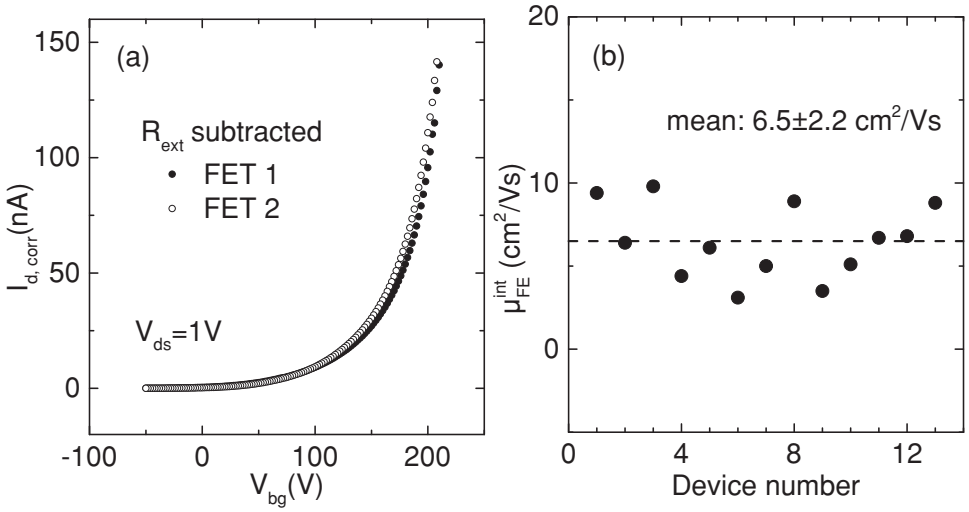

Figure 9. a) Transfer curves ($I_{d,corr}$ vs V_{bg}) at $V_{tg} = 0$ V after subtracting the extrinsic resistance $2R_{ext}$. b) From the slope of the curves in (a), the intrinsic field-effect mobility μ_{FE}^{int} can be estimated for all measured transistors. 13 devices were randomly chosen across the whole die area of >10 cm^2. The yield was 100%.

MoS_2 flakes. The CVD growth of MoS_2 produces characteristic triangular grains with lateral dimensions comparable with exfoliated flakes (few micrometers to 100 μm).[23–26,51] These results are listed in the upper right part of Table 1 (CVD grown MoS_2). The work by Najmaei et al.[23] also claimed the possibility of growing large-area MoS_2 from triangular grains but the resulting films are very non-uniform in thickness (1 layer to more than 4 layers). The reported mobility ranges from 0.02–17 cm^2 V^{-1} s^{-1} for single-layer or few-layer transistors (few l) made from CVD grown triangular grains. Our mobility is close to the upper range of these values, but our devices are made from a continuous large-area film (>10 cm^2) of highly uniform thickness (3 ML ± 0.1 ML). Previously synthesized large-scale films by direct sulfurization of Mo did not show a reliable transistor behavior,[28,29] while the sulfurization of MoO_3 resulted in a relatively low mobility of 0.8 cm^2 V^{-1} s^{-1}.[30] These results are listed in the lower right part of Table 1 (sulfurization of Mo containing films). Based on this comparison, we conclude that our results represent a significant improvement of the MoS_2 synthesis by direct sulfurization of Mo films. Our method provides an excellent combination of large scale growth, extremely high thickness uniformity, and a field-effect mobility comparable with CVD grown MoS_2 grains and exfoliated flakes of similar thickness.

Finally, we would like to address the issue of the mobility estimation in a dual-gated measurement. As has been pointed out by Fuhrer and Hone,[36] several studies strongly overestimated the mobility in a dual-gated setup because the top-gate was left floating (these values are not included in Table 1). The floating top-gate caused an undesired coupling between the back-gate and the top-gate, leading to an incorrect estimate of the back-gate capacitance (and the mobility) by the parallel-plate model. We emphasize that in our setup both gate voltages are well-defined during the measurement. In fact, the contour plot in Figure 8b provides an effective way of measuring the gate coupling ratio. As mentioned above, the measured coupling capacitance ratio in the channel-dominated regime ($s \approx 0.05$) is in excellent agreement with the parallel-plate model, suggesting that our capacitance estimate is correct.

5. Conclusion

In conclusion, we have performed a temperature dependent synthesis study of MoS_2 by direct sulfurization of molybdenum thin films. The final thickness of the material can easily be controlled by adjusting the Mo evaporation rate and time. Using different physical characterization techniques such as XPS, Raman spectroscopy, GIXRD, and cross-sectional STEM, we showed that the structural quality of the synthetic MoS_2 is similar to a bulk geological crystal, if grown at sufficiently high temperatures. In addition, we achieved a highly uniform growth of trilayer MoS_2 with an unprecedented uniformity of ±0.07 nm over a large area (>10 cm^2). Using this highly uniform trilayer film, we fabricated field-effect transistors following a wafer-scale UV lithography process. The yield was 100%. The alumina-coated transistors are virtually hysteresis-free, and show highly reproducible electrical properties. Furthermore, we found that the true electrical performance of the MoS_2 is masked by a large extrinsic resistance at the contact leads. After subtracting the extrinsic resistance, we estimated the intrinsic field-effect mobility to be about 6.5 ± 2.2 cm^2 V^{-1} s^{-1} for transistors made from a continuous trilayer MoS_2 film. To our knowledge, this mobility is among the highest achieved so far using a highly uniform, large-area MoS_2. The electrical performance could be further optimized by reducing the contact resistance and the interface trap density, which is a general challenge for field-effect transistors made from atomically thin semiconductors. Our results represent a significant step towards applications of MoS_2 in transistor-based devices, sensors, and in flexible electronics.

Table 1. Literature values of room temperature field-effect mobility for exfoliated MoS_2 flakes (left) and different growth methods (right). The thickness is given either in numbers of layers (single-layer (sl), bilayer (2l), etc.) or in nm. CVD grown MoS_2 typically forms (isolated) triangular grains with lateral dimensions <100 µm by nucleation growth (upper right). Ref. [23] also showed continuous films but with strong thickness variations (sl – few l). Other growth methods (lower right) use large continuous Mo containing films to directly sulfurize them at high temperatures. Studies marked by * also investigated thickness dependence of mobility. Studies marked by ** account for the effect of the contact resistance.

Exfoliated MoS_2 flakes		
Ref.	Thickness	μ [cm^2 V^{-1} s^{-1}]
[2]	sl	0.5–3
[52]	sl	0.1
[5]	sl	0.2
[53]	sl	10**
[40]	sl	1.1–10
[55]	sl	60
[56]	sl	34
[48]	sl-2l	10–80**
[49]	sl-3l	1–20
[39]	2l	2.4
[58]	2l	0.8
[6]	2l	10–15
[38]	2l	30*,**
[37]	3l	5–7.6
[19]	5–6l (3.5 nm)	19
[41,50]	2 nm	20–30*
[41,50]	13 nm	120–185*
[44]	13 nm	12
[21]	15 nm	30
[59]	30 nm	100
[60]	8–40 nm	10–50
[61]	40–60 nm	15–30

CVD grown MoS_2		
Ref.	Thickness	μ [cm^2 V^{-1} s^{-1}]
[22]	sl-3l	0.02
[26]	sl	2–10
[51]	sl	6–10
[25]	sl	5**
[54]	2l	17
[23]	sl – few l	0.1–10
[24]	few l	1–8
[27]	sl-few l	0.003–0.03
Sulfurization of Mo containing films		
[57]	2l-3l	0.001–4.7
[28]	sl-few l	0.004–0.04
[29]	10 nm	no FETs
[30]	3l	0.8
this work:	3l	6.5

6. Experimental Section

MoS_2 Growth Process: Highly doped silicon wafers were thermally oxidized to create a 300 nm thick SiO_2. Prior to Mo deposition, the substrate was cleaned with organic solvents and piranha solution. Thin Mo films in the range of 1–5 nm were deposited by e-beam evaporation at a rate of 0.3 Å s^{-1}. The samples were then placed into a furnace equipped with a vacuum pump and a gas handling system. After evacuating the chamber, the samples were first annealed in an Ar/H_2 (4:1) atmosphere for 30 min at 300 °C to eliminate possible oxygen contamination. Meanwhile, a separate sulfur container was preheated to 160 °C to generate a sufficient vapor pressure. Afterwards, the chamber was soaked with preheated sulfur gas (20 mTorr) and argon carrier gas (5 Torr). The chamber was heated to the final temperature (between 550 °C and 1050 °C) and left there for 1 h. The chamber was then purged with Ar and cooled down under a constant Ar flow.

Physical Characterization: X-ray photoelectron spectroscopy was performed using a Thermo Scientific K-Alpha XPS system with a monochromated Al Kα X-Ray source and a hemispherical analyzer in Constant Analyzer Energy (CAE) mode (50 eV pass energy, 0.1 eV step size). The X-ray spot size was set to 100 µm.

The Raman spectra were taken with a Renishaw InVia microRaman system using a 532 nm diode laser and 488 nm Ar^+ laser with a 0.25 m focal length spectrometer. The measurements were taken in the 180 degree back-scattered configuration using a 50× objective. Gratings of 1200 l mm^{-1} were used with the 532 nm line and a 3000 l/mm grating was used with the 488 nm line. A spectral resolution of less than 1 cm^{-1}/pixel was obtained with each laser line using a front side illuminated CCD camera.

X-ray diffraction spectra were obtained with grazing incidence X-ray diffractometer (PANalytical X'Pert MRD) with Cu K$^{\alpha}$ operation at 45 kV and 40 mA. A parallel plate collimator was used as diffracted beam optics. The grazing angle was set to 0.5 degree to optimize the signal from the thin film. A continuous scan with 0.05 degree per step size and 0.2 second per step were used.

Cross-Sectional Imaging using STEM: To prepare a cross-section sample of the device using a focused ion beam (FIB) system, protective layers were added to the surface of the sample. A layer of platinum was sputtered using a K575X Emitech coating system. The samples were then placed in an FEI 200TEM FIB system. An additional layer of platinum was FIB-deposited by injection of an organo-metallic gas and rastering the 30 kV gallium ion beam over the area of interest. A thin cross section measuring approximately 15 µm long, 2 µm wide and 10 µm deep was extracted from the die surface using an in situ FIB technique. The cross section was attached to a 200 mesh copper TEM grid using FIB-deposited platinum. One window was thinned to electron transparency using the gallium ion beam of the FEI FIB. To image the cross-sectional sample using a scanning transmission electron microscope (STEM), the grid with the foil was transferred to a Hitachi HD2700 aberration-corrected STEM operated at an accelerating

voltage of 200 kV. Transmitted electron images were acquired at various magnifications in atomic number contrast (Z contrast, or ZC) mode and transmitted electron (TE) mode.

Device Fabrication and Electrical Measurements: The field-effect transistors were fabricated at the wafer scale using a straightforward UV lithography process consisting of several steps. The MoS_2 samples were cleaned with acetone and isopropyl alcohol before each step. First, Ti/Au markers were evaporated using a lift-off process. Second, the MoS_2 layer was etched by a SF_6/O_2 mixture (flow rates: 45 sccm/5 sccm) for 2 min at 20 W power to define the transistor channels. Third, Ti/Au contacts (thickness: 30 nm/30 nm) were formed by a lift-off process. The transistors were measured after this step. Fourth, the whole sample was uniformly coated with 30 nm thick alumina layer, grown by atomic layer deposition (ALD). Last, the Ti/Au top-gate electrodes were deposited using a lift-off process (thickness: 30 nm/60 nm). The transistors were then measured again, with the top gate grounded, to avoid spurious effects due to capacitive coupling between the back gate and the top gate.[36] All electrical measurements were done using a Keithley 4200-SCS parameter analyzer and a CascadeMicrotech probe station at room temperature and ambient conditions.

Acknowledgements

A. T. gratefully acknowledges the financial support by the Swiss National Science Foundation (SNF) within the Early Postdoc.Mobility Program (Grant # P2BSP2_148636). This work was supported by NSF CBET Award #1264705. This work was supported by the Center for Low Energy Systems Technology, one of six centers supported by the STARnet phase of the Focus Center Research Program, a Semiconductor Research Corporation program sponsored by MARCO and DARPA. This work was partially supported by a Georgia Tech Research Institute Robert G. Shackelford Fellowship. The authors thank Corey Joiner for the thermal oxidation of the silicon wafers, Matthew Heidkamp and John Pham of the Georgia Tech Institute for Electronics and Nanotechnology (IEN) for operating the sulfurization furnace, and Tania Roy for fruitful discussions.

Received: April 29, 2014
Revised: June 2, 2014
Published online: August 19, 2014

[1] A. C. Neto, F. Guinea, N. Peres, K. S. Novoselov, A. K. Geim, *Rev. Mod. Phys.* **2009**, *81*, 109.
[2] K. Novoselov, D. Jiang, F. Schedin, T. Booth, V. Khotkevich, S. Morozov, A. Geim, *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 10451.
[3] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, M. S. Strano, *Nat. Nanotechnol.* **2012**, *7*, 699.
[4] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, *ACS Nano* **2014**, *8*, 1102.
[5] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, *6*, 147.
[6] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, T. Palacios, *Nano Lett.* **2012**, *12*, 4674.
[7] F. Perkins, A. Friedman, E. Cobas, P. Campbell, G. Jernigan, B. Jonker, *Nano Lett.* **2013**, *13*, 668.
[8] D. J. Late, Y.-K. Huang, B. Liu, J. Acharya, S. N. Shirodkar, J. Luo, A. Yan, D. Charles, U. V. Waghmare, V. P. Dravid, C. N. R. Rao, *ACS Nano* **2013**, *7*, 4879.
[9] Q. He, Z. Zeng, Z. Yin, H. Li, S. Wu, X. Huang, H. Zhang, *Small* **2012**, *8*, 2994.
[10] H. Li, Z. Yin, Q. He, H. Li, X. Huang, G. Lu, D. W. H. Fam, A. I. Y. Tok, Q. Zhang, H. Zhang, *Small* **2012**, *8*, 63.
[11] J. Z. Ou, A. F. Chrimes, Y. Wang, S. Tang, M. S. Strano, K. Kalantar-zadeh, *Nano Lett.* **2014**, *14*, 857.
[12] B. Liu, L. Chen, G. Liu, A. N. Abbas, M. Fathi, C. Zhou, *ACS Nano* **2014**, *8*, 5304.
[13] D. Sarkar, W. Liu, X. Xie, A. C. Anselmo, S. Mitragotri, K. Banerjee, *ACS Nano* **2014**, *8*, 3992.
[14] L. Wang, Y. Wang, J. I. Wong, T. Palacios, J. Kong, H. Y. Yang, *Small* **2014**, *10*, 1101.
[15] D. Jena, *Proc. IEEE* **2013**, *101*, 1585.
[16] Z. Yin, H. Li, H. Li, L. Jiang, Y. Shi, Y. Sun, G. Lu, Q. Zhang, X. Chen, H. Zhang, *ACS Nano* **2012**, *6*, 74.
[17] R. Sundaram, M. Engel, A. Lombardo, R. Krupke, A. Ferrari, P. Avouris, M. Steiner, *Nano Lett.* **2013**, *13*, 1416.
[18] M. Buscema, M. Barkelid, V. Zwiller, H. S. Zant, G. A. Steele, A. Castellanos-Gomez, *Nano Lett.* **2013**, *13*, 358.
[19] G. A. Salvatore, N. Münzenrieder, C. Barraud, L. Petti, C. Zysset, L. Büthe, K. Ensslin, G. Tröster, *ACS Nano* **2013**, *7*, 8809.
[20] J. Pu, Y. Yomogida, K.-K. Liu, L.-J. Li, Y. Iwasa, T. Takenobu, *Nano Lett.* **2012**, *12*, 4013.
[21] H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu, D. Akinwande, *ACS Nano* **2013**, *7*, 5446.
[22] Y.-H. Lee, X.-Q. Zhang, W. Zhang, M.-T. Chang, C.-T. Lin, K.-D. Chang, Y.-C. Yu, J. T.-W. Wang, C.-S. Chang, L.-J. Li, T.-W. Lin, *Adv. Mater.* **2012**, *24*, 2320.
[23] S. Najmaei, Z. Liu, W. Zhou, X. Zou, G. Shi, S. Lei, B. I. Yakobson, J.-C. Idrobo, P. M. Ajayan, J. Lou, *Nat. Mater.* **2013**, *12*, 754.
[24] A. M. Zande, P. Y. Huang, D. A. Chenet, T. C. Berkelbach, Y. You, G.-H. Lee, T. F. Heinz, D. R. Reichman, D. A. Muller, J. C. Hone, *Nat. Mater.* **2013**, *12*, 554.
[25] W. Zhu, T. Low, Y.-H. Lee, H. Wang, D. B. Farmer, J. Kong, F. Xia, P. Avouris, *Nat. Commun.* **2014**, *5*, 3087.
[26] H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, P. D. Ye, *Nano Lett.* **2013**, *13*, 2640.
[27] Y. Yu, C. Li, Y. Liu, L. Su, Y. Zhang, L. Cao, *Sci. Rep.* **2013**, *3*, 1866.
[28] Y. Zhan, Z. Liu, S. Najmaei, P. M. Ajayan, J. Lou, *Small* **2012**, *8*, 966.
[29] M. R. Laskar, L. Ma, S. Kannappan, P. S. Park, S. Krishnamoorthy, D. N. Nath, W. Lu, Y. Wu, S. Rajan, *Appl. Phys. Lett.* **2013**, *102*, 252108.
[30] Y.-C. Lin, W. Zhang, J.-K. Huang, K.-K. Liu, Y.-H. Lee, C.-T. Liang, C.-W. Chu, L.-J. Li, *Nanoscale* **2012**, *4*, 6637.
[31] C. Wagner, L. Davis, M. Zeller, J. Taylor, R. Raymond, L. Gale, *Surf. Interface Anal.* **1981**, *3*, 211.
[32] C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, S. Ryu, *ACS Nano* **2010**, *4*, 2695.
[33] H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, D. Baillargeat, *Adv. Funct. Mater.* **2012**, *22*, 1385.
[34] M. Chhowalla, G. A. Amaratunga, *Nature* **2000**, *407*, 164.
[35] J. Brivio, D. T. Alexander, A. Kis, *Nano Lett.* **2011**, *11*, 5148.
[36] M. S. Fuhrer, J. Hone, *Nat. Nanotechnol.* **2013**, *8*, 146.
[37] W. Park, J. Park, J. Jang, H. Lee, H. Jeong, K. Cho, S. Hong, T. Lee, *Nanotechnology* **2013**, *24*, 095202.
[38] W. Bao, X. Cai, D. Kim, K. Sridhara, M. S. Fuhrer, *Appl. Phys. Lett.* **2013**, *102*, 042104.
[39] H. Qiu, L. Pan, Z. Yao, J. Li, Y. Shi, X. Wang, *Appl. Phys. Lett.* **2012**, *100*, 123104.
[40] D. J. Late, B. Liu, H. R. Matte, V. P. Dravid, C. Rao, *ACS Nano* **2012**, *6*, 5635.
[41] S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, *Nano Lett.* **2012**, *13*, 100.
[42] A. Cowley, S. Sze, *J. Appl. Phys.* **2004**, *36*, 3212.
[43] J.-R. Chen, P. M. Odenthal, A. G. Swartz, G. C. Floyd, H. Wen, K. Y. Luo, R. K. Kawakami, *Nano Lett.* **2013**, *13*, 3106.
[44] A. Dankert, L. Langouche, V. K. Mutta, S. P. Dash, *ACS Nano* **2014**, *8*, 476.
[45] O. Knopfmacher, A. Tarasov, W. Fu, M. Wipf, B. Niesen, M. Calame, C. Schönenberger, *Nano Lett.* **2010**, *10*, 2268.

[46] A. Tarasov, W. Fu, O. Knopfmacher, J. Brunner, M. Calame, C. Schönenberger, *Appl. Phys. Lett.* **2011**, *98*, 012114.
[47] H. Liu, M. Si, Y. Deng, A. T. Neal, Y. Du, S. Najmaei, P. M. Ajayan, J. Lou, P. D. Ye, *ACS Nano* **2014**, *8*, 1031.
[48] B. W. Baugher, H. O. Churchill, Y. Yang, P. Jarillo-Herrero, *Nano Lett.* **2013**, *13*, 4212.
[49] S. Ghatak, A. N. Pal, A. Ghosh, *ACS Nano* **2011**, *5*, 7707.
[50] S. Das, J. Appenzeller, *Phys. Status Solidi-R* **2013**, *7*, 268.
[51] M. Amani, M. L. Chin, A. G. Birdwell, T. P. ORegan, S. Najmaei, Z. Liu, P. M. Ajayan, J. Lou, M. Dubey, *Appl. Phys. Lett.* **2013**, *102*, 193107.
[52] M.-W. Lin, L. Liu, Q. Lan, X. Tan, K. S. Dhindsa, P. Zeng, V. M. Naik, M. M.-C. Cheng, Z. Zhou, *J. Phys. D: Appl. Phys.* **2012**, *45*, 345102.
[53] B. Radisavljevic, A. Kis, *Nat. Mater.* **2013**, *12*, 815.
[54] W. Wu, D. De, S.-C. Chang, Y. Wang, H. Peng, J. Bao, S.-S. Pei, *Appl. Phys. Lett.* **2013**, *102*, 142106.
[55] D. Jariwala, V. K. Sangwan, D. J. Late, J. E. Johns, V. P. Dravid, T. J. Marks, L. J. Lauhon, M. C. Hersam, *Appl. Phys. Lett.* **2013**, *102*, 173107.
[56] V. K. Sangwan, H. N. Arnold, D. Jariwala, T. J. Marks, L. J. Lauhon, M. C. Hersam, *Nano Lett.* **2013**, *13*, 4351.
[57] K.-K. Liu, W. Zhang, Y.-H. Lee, Y.-C. Lin, M.-T. Chang, C.-Y. Su, C.-S. Chang, H. Li, Y. Shi, H. Zhang, C.-S. Lai, L.-J. Li, *Nano Lett.* **2012**, *12*, 1538.
[58] Y. Li, C.-Y. Xu, B.-Y. Zhang, L. Zhen, *Appl. Phys. Lett.* **2013**, *103*, 033122.
[59] S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, K. Kim, *Nat. Commun.* **2012**, *3*, 1011.
[60] A. Ayari, E. Cobas, O. Ogundadegbe, M. S. Fuhrer, *J. Appl. Phys.* **2007**, *101*, 014507.
[61] W. S. Hwang, M. Remskar, R. Yan, T. Kosel, J. K. Park, B. J. Cho, W. Haensch, H. G. Xing, A. Seabaugh, D. Jena, *Appl. Phys. Lett.* **2013**, *102*, 043116.